ABSTRACT OF THE DISCLOSURE

A data transfer control device and electronic equipment that make it possible to implement high-speed data transfer with reduced overhead processing of firmware and smaller hardware. A data transfer control device that conforms to the IEEE 1394 standard comprises an arbitration circuit that permits firmware (FW) transfer after the completion of one transaction (or one packet transfer) in the continuous packet transfer, if the CPU issues an FW transfer start command during the execution of continuous hardware transfer (HW transfer) processing by a SBP-2 core. If HWStart and FWStart signals go active together, the FW transfer has priority. A header area in RAM is divided into an ordinary header area and an HW header area, and an address generation circuit switches between generating addresses for the ordinary header area and addresses for the HW header area, based on an HWDMARun signal from the arbitration circuit. A data area in RAM is divided into an ORB area and a stream area for the SBP-2 core.